A 14,5 GHz – 0,35 µm frequency divider for dual-modulus prescaler

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Abstract — **This paper reports on structures of frequency divider to be used in the first stage of a dual modulus prescaler. A divider by 2, the prescaler elementary cell, has been designed and characterized. A 4/5 divider is presented as a natural extension of the divider by 2. A first realization has been characterized. We show that an asynchronous structure can overcome the synchronous structure frequency limitations.**

I. INTRODUCTION

Frequency dividers used at high frequency are based on the dual modulus prescaler structure which involves on two stages (Figure 1): the first stage works at high frequency (CML/ECL logic) and allows only two programming ratios (N and N+1), the second stage works at lower frequencies and is fully programmable (CMOS logic). This last stage allows the whole structure to be programmable by controlling the ratio of the first stage.
In this structure, the design difficulty comes from the high-frequency first stage.

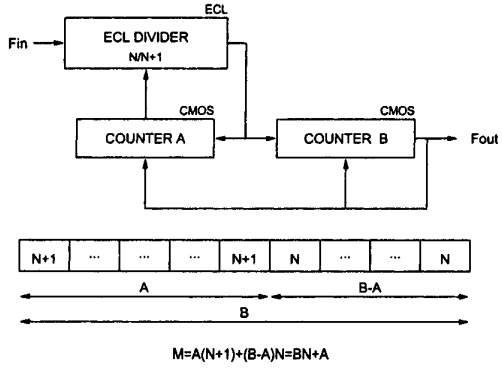

Figure 1: Dual-modulus prescaler principle

About the dual modulus prescaler first stage, a recurrent synchronous structure is usually used but has inherent limitations. This paper proposes an asynchronous circuit which overcomes these limitations and allows operations at a higher frequency.

II. DIGITAL FREQUENCY DIVISION TECHNIQUE

The first frequency divider circuit to be designed is the divider by 2. It is often made with a D-flip-flop (Dff) on which $\overline{Q}$ is connected to D (Figure 2). This Dff is realized with two D-latches (Dl), the first reacting on the high level of the clock, the second on the low level of the clock. The cascade of two D-latches (Dl) turns into a Dff.

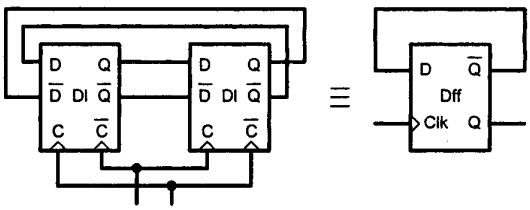

Figure 2: Flip-flop made with two latches

To make a divider by N, the simplest way is to choose N as a power n of two (N=2^n) and to cascade n dividers by 2 in series. The divider by N has therefore the same limitations than the divider by 2. A problem arises when one wants to make the division N+1, because of the "+1". Some additional logic gates are required in order to process this "+1", and they induce further frequency limitation compared to the divider by 2.

A widely used structure is the Johnson divider that is shown in Figure 3.

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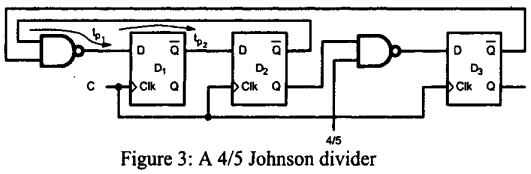

Figure 3: A 4/5 Johnson divider

The D_3 flip-flop allows masking of the loop from Q_2 to D_1 during one period of the clock, making the "+1".

The main drawback of this structure is the propagation delay t_{p1} of the first NAND when the period of the clock is similar to t_{p1}. The divider is not able to work anymore if the signal does not reach at D_1 before the following clock front.

III. DIVIDER BY 2

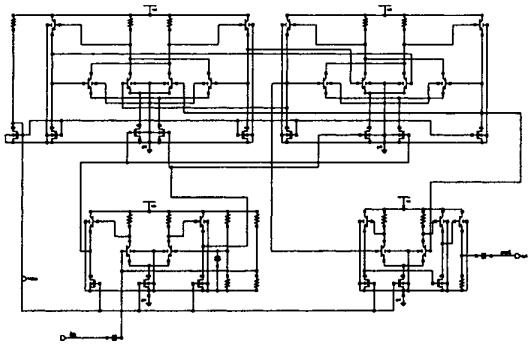
Figure 4 : Divider by 2

Figure 4 shows the ECL implementation of a divider by 2. ECL has been preferred to CML because the NPNs transistors never saturate: they allow a maximum speed. Nevertheless, the ECL emitters followers feature an extra power consumption: one could therefore prefer CML because of this second parameter. In our design (Figure 4), a first stage generates two complementary clocks: the use of two clocks is needed to have a symmetrical behavior in the structure. All the signals are always used with their symmetrical counterpart (D and $\overline{D}$, Q and $\overline{Q}$, C and $\overline{C}$). The output stage allows recombination of the two complementary outputs into a single one. It can't deliver any power and therefore, an output buffer is necessary. Classical ECL logic uses resistors as bias current sources: we decided to use real current sources by using MOS transistors (these MOS devices are used for bias and are not on the path of the high-frequency signals). MOS are also used for the controlled current source on the path of the high-frequency clock: a further improvement in the divider maximum operating frequency could be obtained by the taking over from these MOS by NPNs.

IV. EXPERIMENTAL RESULTS OF DIVIDER BY 2

The circuit has been integrated on a 0,35 µm technology and has been found to work up to 24,5 GHz. Figure 5 shows the minimum and maximum input power needed for the divider satisfactory working. Above 14,5 GHz, the operating power range reduces to a single point : above 14,5 GHz, this divider will not be usable anymore. Paying more attention at the input stage, we can translate this input power sensitivity to lower values. The consumption of the two latches (*i.e.* the flip-flop) is about 3,5 mA.

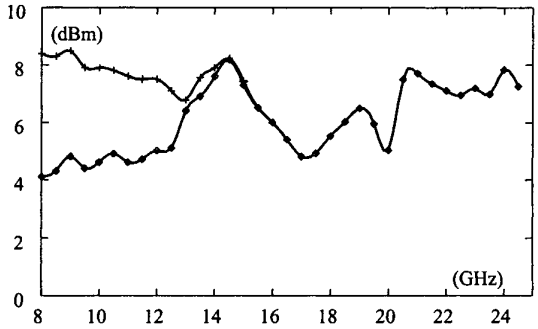

Figure 5 : Input power sensitivity

The available output power is a bit too low (Figure 6), because of an error in the design of the output stage. The simulation shows a typical available output power in the range of $[-10;-5]$ dBm between 6 and 14 GHz that will be obtained with a properly designed buffer.

Because of the digital structure, there is no conversion loss: once the divider synchronized, the output power is unrelated to the input power.

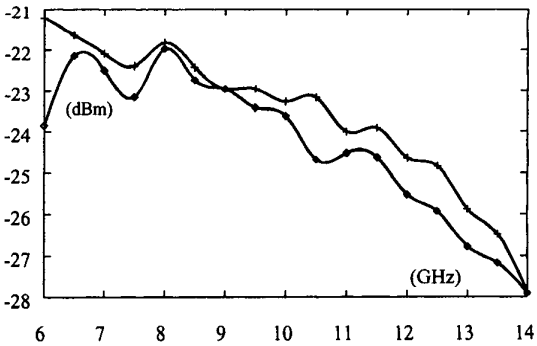

Figure 6 : Available output power for the extrema of acceptable input power

The divider by 2 has shown a frequency of work as low as 700 MHz. Further improvement in the power performance can be achieved in the vicinity of a given frequency (f_0), by adding matching network both at the input (f_0) and the output ($f_0/2$) but at the cost of a reduced working bandwidth.

V. DIVIDER BY 4/5

Most available dual-modulus prescalers are based on the Johnson structure which have inherent limitations with respect to its maximum operating frequency. To overcome its limitations, we propose two original circuits (Figure 7 et 8).

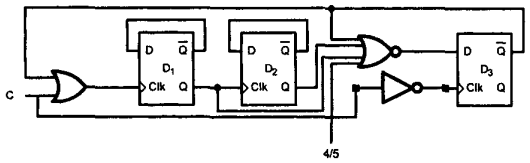

Figure 7 : First schematic

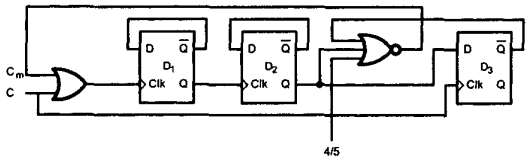

Figure 8 : Second schematic

First of all, all logic gates have been replaced by OR and NOR gates compared to Figure 3, which are the most elementary and fastest structures in CML/ECL logic (NAND or AND are based on OR and NOR plus inverters). Secondly, the gates have been removed from the Q_i-D_j paths, which are the most critical.

The D_3 flip-flop is used to preprocess the initial clock (asynchronous logic), and mask it during one period, freezing the divider during that period in order to achieve the "+1" [1,2]. In the schematic of Figure 8, unlike in the Johnson structure, some other works [3,4,5] or the schematic of Figure 7, there is no logic gates directly connected to the first D-latch: indeed, it is the most critical since it works at the highest frequency.

The second flip-flop works at mid frequency and is therefore less critical, allowing supplementary processing with further logic gates. Yet, if this second flip-flop could not allow other gates to be connected on it, it can be left untouched by using a 8/9 divider instead of a 4/5 one, without decreasing the accuracy of the division ratio (the accuracy is fixed by the "+1"). In the general case of a series of n dividers by 2 (global divider by 2^n), all the flip-flops from 1 to $n-1$ are left untouched until the n^{th} flip-flop works at a frequency sufficiently low to allow further processing.

Moreover, the work of the divider is ensured if the masking is done each N periods (in fact N+1 periods), anywhere it occurs: thus the propagating delay t_p from Q_3 output to the OR input (currently the propagating delay through the NOR gate) is not of importance, it is only the width t_l of the masking pulse which is needed to be equal to the clock period (Figure 9).

Therefore a critical path delay has been transformed into a non-critical path delay [6].

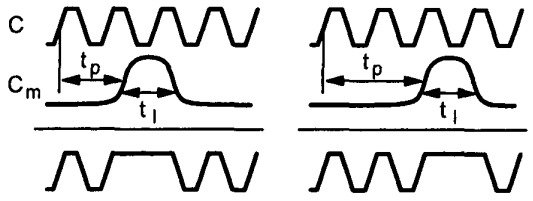

Figure 9 : Illustration of non-critical path

A case of dysfunction could arise if the masking pulse is exactly aligned with the clock pulse. One can avoid this by simply adding an appropriate delay on the path.

From this approach, we can predict the work of a divider N/N+1 from that of a divider by 2.

At this point, it must be said that the divider by 2 configuration is the best way to test a flip-flop because it is a very symmetrical connection that equilibrates the structure. This complete symmetry is a great benefit at high frequencies. The D_3 flip-flop in our design is not configured as a divider by 2. Its structure is the same as D_1 and D_2 (symmetrical) but there is no feedback further equilibrates it: D_3 will not work at the speed given by that of its divide-by-2 configuration. It is therefore more exact to say that the 4/5 divider 's speed will be comparable to the D flip-flop 's.

VI. RESULTS OF THE 4/5 DIVIDER

The structure of Figure 7 has already given results. It is based on the same principle of using non-critical paths for processing the "+1", but currently use the output of all the flip-flop to make a 0-detect [1] which appears each N+1

period and causes a masking of one period: the first flip-flop is therefore under influence and shall behave at a lower speed than the divider by 2.

This circuit (Figure 7) has been simulated to operate at a frequency of 10 GHz with the same acceptable input and available output similar to divider by 2 results (input and output stages are the same).
The measurements of the input (light gray) and output (dark gray) powers are shown in Figure 10.

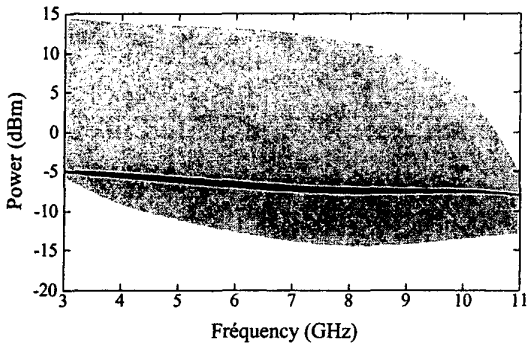

Figure 10°:Input and output power bandwidths according to input frequency

It must be enlightened that:

- The maximum operating frequency of the 4/5 divider is 11 GHz.
- Several dividers of the same kind can be cascaded together if the output power operating range is included in the input one.

Although, these results are already relevant, we feel that this structure has inherent limitations owing to the signal taking after each divider by 2 and the four input NOR gate; that can be overcame with the improved design on the Figure 8.

Available results are already interesting. We are now expecting further experimental results from the structure of Figure 8.

VII. Conclusion

We have reported the design of the first stage of a high-frequency dual modulus prescaler. A divider by 2 has been extensively reviewed and a original 4/5 divider structure has been proposed as a natural extension of the divider by 2. The circuit is based upon an asynchronous logic which overcomes the frequency limitations of the classical synchronous design.

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